

Customer No.: 31561
Application No.: 10/605,254
Docket No.: 9676-US-PA

IN THE SPECIFICATION

Please amend the specification as follows.

At paragraphs [0013]-[0014] of page 2.

[0011] Figures 2A to 2G are cross-sectional views along line ~~1-1~~ 1-1' as shown in Figures 1A to 1G, respectively.

[0012] Figures 1A to 1G are top views showing the fabrication process of a flash memory according to a preferred embodiment of the present invention. Figures 2A to 2G are cross-sectional views along line ~~1-1~~ 1-1' as shown in Figures 1A to 1G, respectively. Referring to Figures 1A and 2A, a substrate 100 is provided. The substrate 100 includes a silicon substrate, for example. A tunneling dielectric layer 102, a conductive layer 104 and a mask layer 106 are sequentially formed on the substrate 100. The material of the tunneling dielectric layer 102 includes silicon oxide, and the thickness thereof is about 50 angstroms to about 100 angstroms, for example.